**Traffic Signal Controller**

**Specification:**

* The traffic signal for main highway gets the highest priority because cars are continuously present on the highway. Thus, the main highway signal remains green by default.
* Occasionally cars from the country road arrive to traffic signal. The traffic signal for country road must turn green only long enough to let the cars on the country road go.

A cross with text on it

Description automatically generated

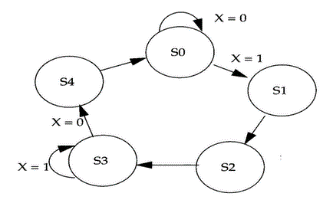
* As soon as there are no cars on the country road, the country road traffic signal turns yellow and then red and traffic signal on main highway turns green again.
* There is a sensor to detect cars waiting on the country road. The sensor sends a signal X as input to controller. X=1 if there are cars on the country road, otherwise x=0
* There are delays on transition from S1 to S2, from S2 to S3 and from S4 to S0. The delays must be controllable

Problem: Build a Verilog model for traffic signal control using state machine

State table

|  |  |
| --- | --- |
| State | Signals |
| S0 | Hwy = Green, Cntry = Red |
| S1 | Hwy = Yellow, Cntry = Red |
| S2 | Hwy = Red, Cntry = Red |
| S3 | Hwy = Red, Cntry = Green |
| S4 | Hwy = Red, Cntry = Yellow |

State diagram



Block diagram of traffic signal controller

Input X,

Output Hwy, Cntrl

Clock for sequential circuit and

Clear to go to default state